DOUBLE-GATE FET WITH PLANARIZED SURFACES AND SELF- ALIGNED SILICIDES

ABSTRACT

It is, therefore, an object of the present invention to provide a structure and method for an integrated circuit comprising a first gate, a second gate, and source and drain regions adjacent the first and second gates, wherein the structure has a planar upper structure and the first gate, source and drain regions are silicided in a single self-aligned process (salicide).